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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/612,971	07/10/2000	Jae-seong Shim	1293.1128/MJB	9406

21171 7590 09/27/2002

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EXAMINER
TU, CHRISTINE TRINH LE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/612,971	SHIM ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 29-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claim invention is recited with an error correction block embodied on a recording medium (which is an optical disk). However, the data does not impart functionality to either the data as claimed or to the optical disk. As such, the claimed invention is recited with non-functional descriptive material, i.e., mere data. Non-functional descriptive material stored on a recording medium is merely carried on the medium, it is not structurally and functionally interrelated to the medium.

3. Claims 1-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a.Claim 1:

At lines 5-6, the phrase "(here, x is an integer equal to or greater than 2)" is unclear. It should be replaced with -- where in x is an integer equal to or greater than 2. This is because the use of parenthesis "( )" should be avoided and it is not clear whether the phrase therein is actually recited in the claim.

b.Claim 2:

At lines 1-2, the phrase "the PIs are Reed-Solomon signs" cannot be understood. What are Reed-Solomon signs ? How the inner parities (PIs) can be Reed-Solomon signs?

c.Claim 10:

At lines 3 and 4, the term "Pis" should be replaced with --PIs--. In other words, consistency of each term should be used throughout the claims.

d.Claim 15:

At lines 3-4, it is not clear where the data frame comes from?

The step of "form a data frame" is not coherent with the steps previously recited (in claim 1); this step appears to be not interrelated the others.

e.Claim 17:

At lines 1-2, is there any interrelationship between the Galois Field (GF) performance and the parities (PI) or (PO)?

What is "GF(28)"? Again, the use of parenthesis "( )" should be avoided and it is not clear whether the number therein is actually recited in the claim.

f.Claims 3-9, 11-14, 16 and 18:

These claims are rejected because they depend on claim(s) 1, 2 and 10 and contain the same problems of indefiniteness.

4. The following rejections are based on the best understanding of the claimed invention by the examiner in view of the ambiguities that exist in the claims as mentioned above (supra ¶ 3).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-9, 15-16, 18-27 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (6,252,838 and Kuroda hereinafter).

Claim 1:

Kuroda discloses the invention substantially as claimed. Kuroda teaches (figures 1A & 1B) an error correcting process for generating an ECC block from a data structure. The data structure is segmented into a plurality of data sectors (20). Each section (20) is firstly divided into plural blocks each of which is 172 bytes data (figure 1B) and each divided data is arranged in a vertical direction. At this time, the data blocks (33) are arranged in 12 lines in the vertical direction (column 5 lines 27-50).

Kuroda also teaches that for each data block (33) arranged in the vertical direction, ECC internal code (PI) (31) having 10 bytes data is affixed to the end of the data block (33) to constitute one correction block (34). At this stage, the ECC internal codes (31) (PIs) are affixed and arranged in the vertical direction. After that, this process is repeated with respect to 16 data sectors (20) (column 5 lines 51-59).

Kuroda further teaches that the correction block (34) of 192 lines are divided in the vertical direction from the beginning thereof, for each one byte, in the state that the 192 Ines of the correction blocks (34) are arranged in the vertical direction. 16 ECC external codes (PO) (32) are affixed to each of the vertically divided data blocks, It is noted that ECC external code (PO) (32) is also affixed to a portion of the ECC internal code (PI) (31) within the correction block (34) (column 5 lines 60-57).

Kuroda does not explicitly teach the features of generating PIs and POs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's error correcting process would have been comprised of the features of generating the POs and POs. The artisan would have been motivated to realize so because Kuroda teaches that each of the PIs and each of the POs is being obtained and affixed to the end of a data block (33) and a vertically divided data blocks, respectively (column 5 lines 51-67).

Claims 2-6 and 16:

Kuroda does not explicitly teach $(n/x) + e > 256$, $(n+e) \times (m+f) < 64K$, $n=688$ and $m=96$, $x=172$ and $e=8$, nor $f=12$. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's value of variables m, n x, e and f would have been quality the situations above. The artisan would have been motivated to do so because choose the values of m, n, x, e and f would have been obvious of design choice for the size of each data sector and size of each ECC block.

Claims 7-9 and 18:

Kuroda teaches that an encoder (9) affixes the ECC internal code (PI) (31) and ECC external code (PO) (32) to constitute the ECC block (30) including the interleave process to the ECC block (30) (column 8 lines 14-18).

Claim 15:

Kuroda teaches that a data sector comprises 4-byte ID, 2-byte IEC, 6-byte RSV, 2048-byte data, and 4-byte EDC (figure 1A).

Claims 19-22:

Kuroda discloses the invention substantially as claimed. Kuroda teaches (figures 1A & 1B) an error correcting process for generating an ECC block from a data structure. The data structure is segmented into a plurality of data sectors (20). Each section (20) is firstly divided into plural blocks each of which is 172 bytes data (figure 1B) and each divided data is arranged in a vertical direction. At this time, the data blocks (33) are arranged in 12 lines in the vertical direction (column 5 lines 27-50).

Kuroda also teaches that for each data block (33) arranged in the vertical direction, ECC internal code (PI) (31) having 10 bytes data is affixed to the end of the data block (33) to constitute one correction block (34). At this stage, the ECC internal codes (31) (PIs) are affixed and arranged in the vertical direction. After that, this process is repeated with respect to 16 data sectors (20) (column 5 lines 51-59).

Kuroda further teaches that the correction block (34) of 192 lines are divided in the vertical direction from the beginning thereof, for each one byte, in the state that the 192 Ines of the correction blocks (34) are arranged in the vertical direction. 16 ECC external codes (PO) (32) are affixed to each of the vertically divided data blocks, It is noted that ECC external code (PO) (32) is also affixed to a portion of the ECC internal code (PI) (31) within the correction block (34) (column 5 lines 60-57).

Kuroda does not explicitly teach the features of generating PIs and POs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Kuroda's error correcting process would have been comprised of the features of generating the POs and POs. The artisan would have been motivated to realize so because Kuroda teaches that each of the PIs and each of the POs is being obtained and affixed to the end of a data block (33) and a vertically divided data blocks, respectively (column 5 lines 51-67).

Claims 23-27:

Kuroda teaches that an encoder (9) affixes the ECC internal code (PI) (31) and ECC external code (PO) (32) to constitute the ECC block (30) including the interleave process to the ECC block (30) (column 8 lines 14-18).

Claims 29-34:

Kuroda teaches a ECC block is being recorded on a DVD. The ECC block comprises inner parities (PIs) and external parities (POs) that are affixed and arranged in the vertical direction and in the horizontal direction (figures 1A & 1B, column 1 lines 7-13, column 6 lines 13-33 and column 5 lines 27-67).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Ozaki et al. (4,719,628).

Claim 17:

Kuroda does not teach the Galois Field operation. Ozaki teaches that Galois field GF (2^m) can be used in error correction method.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Ozaki's Galois Field method in Kuroda's error correcting process. One having ordinary skill in the art would be motivated to combine the teachings of Kuroda and Ozaki because both references teach error correction for data information.

9. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (6,252,838) in view of Hoshino (5,586,108).

Claim 28:

Kuroda does not teach the feature of interleaving quantity of the data in relation to the size of a burst error. Hoshino, however, teaches that the length of burst error correction of data is increased by interleaving error correction code among the sectors (abstract, lines 8-10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to Kuroda's interleaving feature would have considered the burst error correction as taught by Hoshino. One having ordinary skill in the art would be motivated to combine the teachings of Kuroda and Hoshino because both of the references teach an error correction method being used in a disk recording medium.

10. Claims 10-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. L. Tu whose telephone number is (703) 305-9689. The examiner can normally be reached on Monday to Thursday from 8:30 A.M. to 6:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

13. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

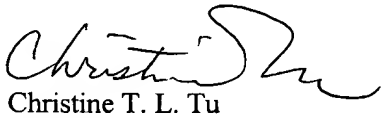
or faxed to:

(703) 746-7238 (for formal after-final communications intended for entry),
(703) 746-7239 (for formal communications intended for entry),

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. 22202, Sixth Floor (Receptionist).



Christine T. L. Tu
Primary Patent Examiner
Art Unit 2133

September 25, 2002